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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,007	02/17/2005	Kazuhisa Arai	2005_0208A	1754

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EXAMINER

WILCZEWSKI, MARY A

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/525,007

Applicant(s)

ARAI, KAZUHISA

Examiner

M. Wilczewski

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 17 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 February 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 17.02.2005
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Priority*

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 6-8 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hitachi Ltd. JP 2002-075940, cited by Applicant.

Hitachi Ltd. discloses a method for fabricating a semiconductor wafer which comprises integrating a glass supporting substrate with a semiconductor wafer wherein the wafer is stuck to the supporting substrate through an adhesive containing resin (see paragraphs [0031]-[0034], [0042]-[0043] and [0069]-[0077] and figures 2 and 10); thinning the back surface of the wafer by grinding the wafer to a thickness of 70 or 100 micrometers (see paragraphs [0045] and [0059], respectively, and figure 11); and forming a conductive film on the back surface of the wafer by sputtering (see paragraphs [0059]-[0065] and figure 11).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hitachi Ltd., JP 2002-75940, as applied to claim 1 above, further in view of Watanabe et al., US Patent 5,429,711.

Hitachi Ltd. is applied as above. Hitachi Ltd. clearly teaches to thin the back surface of the wafer by grinding, see paragraphs [0045] and [0059]. Hitachi Ltd. lacks anticipation only of the particulars of the thinning device (claim2), that is, that the thinning device has at least one chuck table for holding the wafer, and that the device is a polishing device (claim 4). Watanabe et al. disclose a wafer manufacturing method in which the back surface of a wafer is thinned using a polishing machine, see col. 5, lines 22-30. The wafer is fixedly placed on the polishing plate (chuck table) of a polishing machine. In light of the disclosure of Watanabe et al., it would have been obvious to one skilled in the art that a polishing machine could be used in the known method of Hitachi Ltd., and it would have been further obvious that the wafer would need to be held on the polishing plate (chuck table) of the polishing device in order to thin the back surface of the wafer.

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hitachi Ltd., JP 2002-75940, as applied to claim 1 above, further in view of Wolf et al., Silicon Processing for the VLSI Era, Volume 1-Process Technology, pages 331-365.

Hitachi Ltd. is applied as above. Hitachi Ltd. clearly teaches a film formation step in which a conductive film is formed on the back surface of the thinned wafer integrated with the supporting substrate by sputtering, see paragraphs [0059]-[00661]. Hitachi Ltd. lacks anticipation only of the particulars of the sputtering apparatus used, that is, that the sputtering apparatus operates at a reduced pressure (claim 5) and that the apparatus has a holding portion on which the integrated semiconductor wafer is held (claim 3). Wolf et al. disclose that sputtering is performed at reduced pressures, see, for example, page the bottom of page 331. Wolf et al. also show examples of typical sputtering apparatuses which all comprise substrate supports, see, for example, figure 19 on page 352 or figure 26 on page 360. It is well within the purview of thw skilled artisan to recognize from the disclosure of Wolf et al. that the sputtering film-forming process used in the known method of Hitachi Ltd. is performed at reduced pressures and that during the sputtering process the integrated wafer of Hitachi Ltd. would be placed on a substrate holding portion (support).

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited references to Beyer et al., Ghyselen et al.,

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and Cheng et al. disclose various methods of bonding substrates and removal of one of the bonded substrates. Jeong discloses a CMP apparatus and a method for its use.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Wilczewski whose telephone number is (571) 272-1849. The examiner can normally be reached on Monday and Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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